DRY PLASMA ETCHING FOR MICRO

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DRY PLASMA ETCHING
FOR MICRO-PATTERNING ONTO THE DLC COATING

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ABSTRACT

Micro-patterning has become a new keyword in the industries; e,g, designed micro-textures are imprinted on to the micro-electronic devices, sensors, optics, molds and dies. Among several methods using wet and dry etching processes, high density oxygen plasma etching process has been developed. This process is characterized by no use of hazardous solvents, high controllability in etching, uniformity in etching and high resolution. In the present paper, micro-patterning behavior is described by using the DLC-coated silicon wafer. Micro-grooves and micro-grids are uniformly formed onto the DLC coating with highly accurate dimensions and depth profile. Reactive ion etching behavior is discussed in this micro-grooving with different groove widths. Plasma etching process is optimized to control this local etching process both in micro-grooving and micro-gridding.

1. INTRODUCTION

Micro-patterning has become a new keyword in the industries. Micro-electric devices, sensors, and optical elements require for designed micro-textures on their surfaces to be imprinted by micro-forming with micro-textured molds and dies (Kim, 2012).

Several methods have been developed for this micro-patterning. Micro-patterns were successfully formed by the high density oxygen plasma etching on the DLC layer with the thickness of 5 μm; SKD11 mold-die with micro-patterned DLC coating was used to duplicate this micro-pattern onto polymer and glass products via the mold-stamping (Aizawa, 2011). Nano-imprinting processes were also effective to make micro- and nano-patterns onto polymer sheets or thin metallic substrates (Guo, 2007; Kim, 2012).

In this study, two dimensional masking is prepared onto the DLC coating; the initial mask is made from resin and oxide layers on the silicon (Si) substrate by using the chemical etching process. High density oxygen plasma etching is applied to make dry etching for fine three dimensional micro-patterning. The effect of processing parameters onto this etching behavior is discussed to search for optimum processing parameters.

2. EXPERIMENT

Our developing high density RF-DC plasma etching system was first introduced. Different from the conventional plasma etching, no chemical agents are utilized in this process. DLC-coated test-piece was used to measure the removal rate. DLC-coated silicon sample with initial micro-pattern was also used to describe the oxygen plasma etching behavior.

2.1 Plasma Etching System

Plasma etching system used in this experiment is shown in Fig. 1. In this etching process, only pure oxygen gas is used to remove the DLC coating. This system has three main processing parameters: i.e. RF-voltage, DC-bias and oxygen gas pressure. In parallel with these parameters, experimental set-up has influence on the etching process; e.g. spatial position of dipole electrode to generate RF-plasmas, distance between this electrode and cathode, and distance between the substrate electrode. Typical experimental set-up is depicted in Fig. 2. In the following plasma etching experiments, the above parameters are varied to find the optimal feasible range in those parameters for efficient removal of DLC coating. Under optimum selection of parameters, micro-patterning is performed to describe the etching behavior. This machine has the following characteristics with radio frequency (RF) working around 2 MHz. This RF-plasma is directly controlled by its voltage from 60 V to 250V DC bias is also controllable from 0V to 600V. The pressure is varied from 10 Pa to 100 Pa with automatic gas flow rate control. In this study, the parameters were varied as follows; the RF voltage is varied in the range of 200V to 250 V, DC-bias,-400V to 600 V and gas pressure, 20 Pa to 40 Pa. Base pressure was below 0.1 Pa.

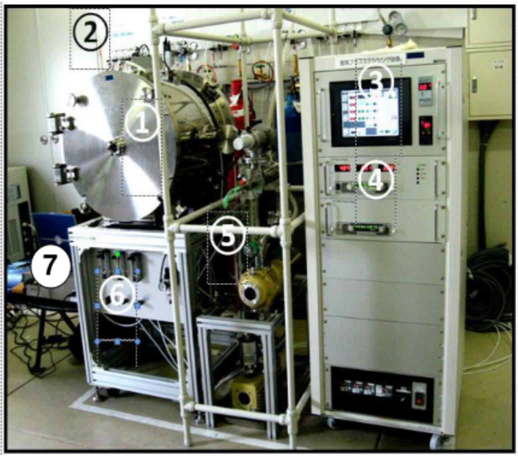


Fig. 1: High density plasma etching system. 1: Chamber, 2: RF-plasma generator, 3: Control-panel, 4: Electric sources, 5: Evacuation system, 6: Gas supply, 7: Plasma Diagnosis (PMA-11)

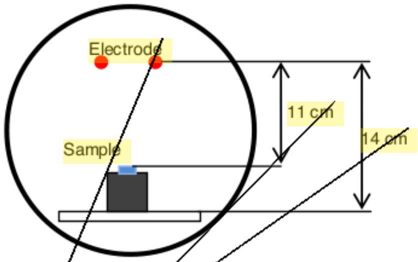
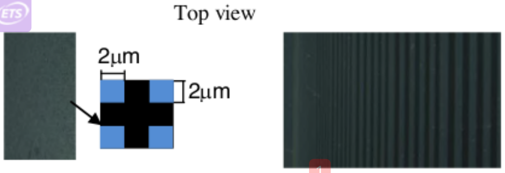


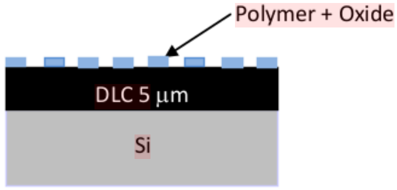
Fig. 2: A Typical experimental set-up for plasma etching

2.2 Sample

The sample used in experiment is shown in Fig. 3.



a. Grid pattern b. Line pattern



c. Side view.

Fig. 3: Geometric configuration of samples.

Silicon wafer was employed as a substrate, and, subsequently DLC coating and polymer oxide mask were stacked onto it. The thickness of silicon wafer, DLC coating and oxide mask were 0.525 mm, 5 μm and 1.2 μm, respectively. There are two kinds of micro patterns: micro-grids and micro-lines. Grids pattern have a size of 2 x 2 μm as shown in Fig 3a). The width of line pattern varies in a series of 3, 4, 5, 7, 10, 20, 30, 50, 70 and 100 μm in Fig. 3b).

3. RESULTS AND DISCUSSION

The etching rate was defined by the ratio of the removed DLC thickness to the removal time required. The plasma etching process worked optimally on RF-voltage of 250 V, DC bias, -400 to -600V and the pressure, 20 Pa. The etching rate ranged over 1.193 to 1.633 nm/s. It is used for further research to remove the DLC coating with thickness of 5 μm.

3.1 Line Pattern

Laser reflection profilometer (Lasertec HD 100) was employed to measure the micro-line pattern. Fig. 4 and Fig. 5, depicted the depth profile of etched DLC-coated sample under the processing condition where the RF-voltage was 250 V, the DC-bias, -600 V, the pressure, 20 Pa and the duration time, 3000s. Remembering that the initial DLC coating thickness was 5 □m, the original DLC coating in the un-masked regions was completely removed. In addition, the flat surface of DLC coating before etching was successfully wrought to a micro-grooved DLC coating, irrespectively of the micro-line widths down to 20 □m. When the initial line width is less than 20 □m, the micro-groove pattern becomes away from the step-wise depth profile, as seen in the micro-grooves at the left-hand side of Fig. 5. This irregularity might come from the micro-etching process in the narrowed channels in the masking.

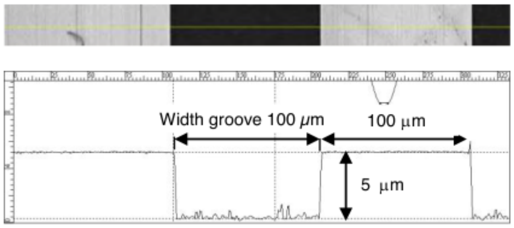


Fig. 4: Depth profile of etched sample by using the wider line-patterned mask in case where RF-voltage was 250 V, the DC bias, -600 V, the pressure, 20 Pa, and the duration time, 3000s.

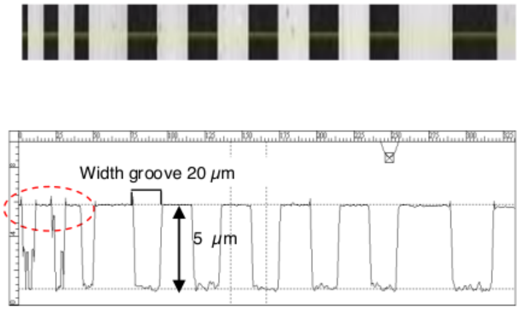


Fig. 5: Depth profile plasma etching by using the narrower line-patterned mask in case where the RF-voltage was 250 V, the DC bias, -400 V, the pressure, 20 Pa and the duration time, 4000s.

3.2 Grid Pattern

Optimized processing parameter was used to make micro-grid patterning onto DLC-coating. Figure 6 depicted the SEM cross-sectional view of grid-pattern sample after etching.

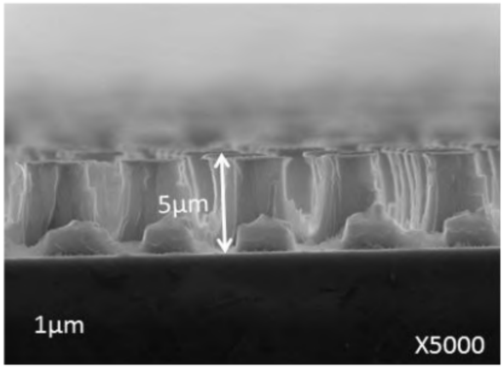


Fig. 6: SEM image of etched sample by RF (250 V), DC-bias (-600 V), pressure (20 Pa), Time (3000s).

In general, higher DC-bias and lower pressure drive the etching process to be enough strong to make severe damage even to DLC coating. In fact, as seen in Fig. 6, etched columns were timbered or broken after etching. On the other hand, the duration time to perfect removal of DLC coating in the un-masked regions must be significantly delayed by much reduction of DC-bias and increase of pressure. Here, only the duration time was reduced from 3000 s to 2000 s as the first remedy to reduce the damage onto DLC coating. Figure 7 depicted the SEM cross-sectional image of etched sample by new processing conditions. Damages to DLC columns were minimized by this change of duration time in etching.

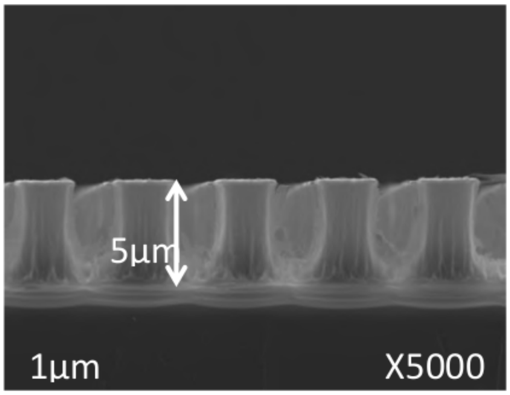


Fig. 7: Fig. 6: SEM image of etched sample by RF (250 V), DC-bias (-600 V), pressure (20 Pa), Time (2000s).

4. DISCUSSION

From the all cross-sectional views of the grid-pattern sample by SEM, micro-etching process must be reconsidered to be free from irregular shaping in micro-patterning. In particular, over-etching comes from excess etching time and faster reactive ion etching (RIE).

Final determination of plasma etching process must be considered. Even after the DLC coating is removed completely, oxygen ions (O) maintain to bombard on the silicon substrate with no reaction. Then ions (O) tend to bounce off the side walls of DLC coating. Due to oxygen ion bombardment onto the sidewalls of DLC (C), carbon is eroded by the reaction between O and C in DLC to form CO, to be ejected out of chamber by a vacuum pump. In this manner, over-etching is induced by this bombardment.

Regarding the problems mentioned above, it is necessary to utilize the in-situ plasma diagnosis to investigate what occurs during the plasma etching process. Remembering that the spectrum of CO peak appears at wavelength of 256.83 nm after Ref. (Aizawa, 2012), we can predict what occurs during the etching process. Etching process has been completed when the intensity of measured CO peak is minimized.

The etching parameters above result in very fast RIE. It is characterized by relatively rapid etching rate (Redationo, 2011). RIE were quickly affected by ion density and movement of oxygen ions. Oxygen ions are very fast to get into the groove below 20 μm width so that collisions between ions become more frequent and the ion cannot vertically bombard onto DLC surface. Consequently, all groove-pattern under the width of 20 μm is not perfectly etched, resulting in the cone-like shape. The plasma etching in the groove size over 20 μm is performed perfectly. That is, it is proved oxygen ions easily enter and exit through this pattern during bombardment onto DLC coating.

To solve this problem, the absolute control of plasma etching parameters has to be considered; i.e. movement of the ions can be slowed by reducing the ion density. This can be done by increasing the gas pressure, and lowering the RF power and DC bias. In order for the proper analysis to determine the density and movement of oxygen ions during the etching process in the chamber, Langmuir probe is indispensable for the system. With the help of Langmuir probe, some important plasma parameters are obtained, such as electron density, electron temperature, plasma potential, floating potential and so on. From the available data, the kinetic energy of the ion is calculated so that it can estimate the movement of oxygen ions and density.

5. CONCLUSION

Plasma etching has successfully created a micro-grid-patterned (2 x 2 μm^2) DLC coating with the thickness of 5 μm on silicon substrate. Over-etching can be overcome with appropriate selection of duration time and processing parameters controlling plasma etching.

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